CLAIMS

What is Claimed is:

1. A content addressable memory (CAM) cell comprising:

a static random access memory (SRAM) cell that operates in response to a V_{CC} supply voltage, the SRAM cell storing a data value;

a first set of one or more bit lines coupled to the SRAM cell, wherein the data value is written to and read from the SRAM cell on the first set bit lines, the first set of bit lines having a signal swing equal to the V_{CC} supply voltage; and

a second set of bit lines coupled to receive a comparison data value, the second set of bit lines having a signal swing less than the V_{CC} supply voltage.

2. The CAM cell of Claim 1, further comprising a circuit for comparing the data value with the comparison data value to determine whether a match exists.

3. The CAM cell of Claim 2, wherein the circuit comprises:

a first transistor having a gate coupled to receive a signal representative of the data value; and

a second transistor having a gate coupled to receive a signal representative of the inverse of the data value.

4. The CAM cell of Claim 3, wherein the second set of bit lines comprises:

a first bit line coupled to a source region of the first transistor; and

a second bit line coupled to a source region of the second transistor.

5. The CAM cell of Claim 4, wherein a drain region of the first transistor is coupled to a drain region of the first transistor at a first node.

6. The CAM cell of Claim 5, further comprising a diode element coupled to the first node.

7. The CAM cell of Claim 6, further comprising a local mask transistor coupled in series with the diode element.

8. The CAM cell of Claim 6, wherein the diode element comprises a diode-connected transistor.

9. The CAM cell of Claim 6, wherein the diode element comprises a P-N junction.

10. The CAM cell of Claim 6, further comprising a match line coupled to the diode element, wherein the diode element is forward biased from the match line to the first node.

11. The CAM cell of Claim 10, wherein the match line has a signal swing equal to a transistor threshold voltage.

12. The CAM cell of Claim 10, further comprising a sensor circuit coupled to the match line, the sensor circuit pre-charging the match line to a voltage less than the V_{CC} supply voltage.

13. The CAM cell of Claim 12, wherein the sensor circuit comprises a logic gate for providing an output signal that indicates whether a match or a no-match condition exists, the output signal having a signal swing equal to the V_{CC} supply voltage.

14. The CAM cell of Claim 1, further comprising a bit line control circuit for biasing the second set of bit lines.

15. The CAM cell of Claim 14, wherein the bit line control circuit comprises a first transistor for connecting the second set of bit lines during a pre-charge operation.

16. The CAM cell of Claim 14, wherein the bit line control circuit comprises one or more transistors for connecting the second set of bit lines to a voltage supply line during a global masking operation, the voltage supply line having a voltage less than the V_{CC} supply voltage.

17. The CAM cell of Claim 14, wherein the bit line control circuit comprises a plurality of transistors for selectively coupling the second set of bit lines to a voltage supply line and a ground supply line, whereby the second set of bit lines receive voltages representative of

the comparison data value from the voltage supply line and the ground supply line, the voltage supply line having a voltage less than the V_{CC} supply voltage.

18. The CAM cell of Claim 17, wherein the voltage supply line has a voltage of two times a transistor threshold voltage.

19. The CAM cell of Claim 14, wherein the bit line control circuit is powered by a supply voltage less than the V_{CC} supply voltage.

20. A content addressable memory (CAM) cell having a match line that carries a signal to indicate whether a match or a no-match condition exists within the CAM cell, ~~the match line having a signal swing~~ wherein the difference between a voltage on the match line during the match condition and a voltage on the match line during the no-match condition is equal to one transistor threshold voltage.

21. A method of operating a content addressable memory (CAM) cell that includes a static random access (SRAM) cell, the method comprising the steps of:

operating the SRAM cell in response to a V_{CC} supply voltage, the SRAM cell storing a data value;

writing a data value to the SRAM cell on a first set of one or more bit lines, the first set of bit lines having a signal swing equal to the V_{CC} supply voltage;

reading data values from the SRAM cell on the first set of bit lines;

controlling the signal swing on the first set of bit lines to be equal to the V_{CC} supply voltage;

providing comparison data values to the CAM cell on a second set of bit lines; and

controlling the signal swing on the second set of bit lines to be less than the V_{CC} supply voltage.

22. The method of Claim 21, further comprising the step of comparing the data value stored in the CAM cell with the comparison data value to determine whether a match condition or a no-match condition exists.

23. The method of Claim 22, further comprising the step of indicating a match condition and a no-match condition by providing a signal having a signal swing equal to one transistor threshold voltage.

24. The method of Claim 22, wherein the step of comparing comprises the step of coupling one of the bit lines in the second set of bit lines to a match line in response to the data value stored in the CAM cell.

25. The method of Claim ~~24,~~ further comprising the step of pre-charging the match line to a voltage less than the V_{CC} supply voltage.

26. The method of Claim 25, further comprising the step of discharging the match ~~line~~ when a no-match condition exists.

27. The method of Claim 23, further comprising the step of converting the signal ~~having~~ the signal swing of one transistor threshold voltage to a signal having a signal swing equal to the V_{CC} supply voltage.

28. The method of Claim 21, further comprising the step of equalizing the second set of bit lines prior to providing the comparison data values to the CAM cell on the second set of bit lines.

29. The method of Claim 21, further comprising the step of connecting the second set of bit lines to a voltage supply line during a global masking operation, the voltage supply line having a voltage less than the V_{CC} supply voltage.

30. The method of Claim 21, further comprising the step of selectively coupling the second set of bit lines to a voltage supply line and a ground supply line, whereby the second set of bit lines receive voltages representative of the comparison data value from the voltage supply line and the ground supply line, the voltage supply line having a voltage less than the V_{CC} supply voltage.

31. The method of Claim 30, wherein the voltage supply line has a voltage of two times a transistor threshold voltage.

32. The method of Claim 21, further comprising the step of biasing the second set of bit lines with a supply voltage less than the V_{CC} supply voltage.